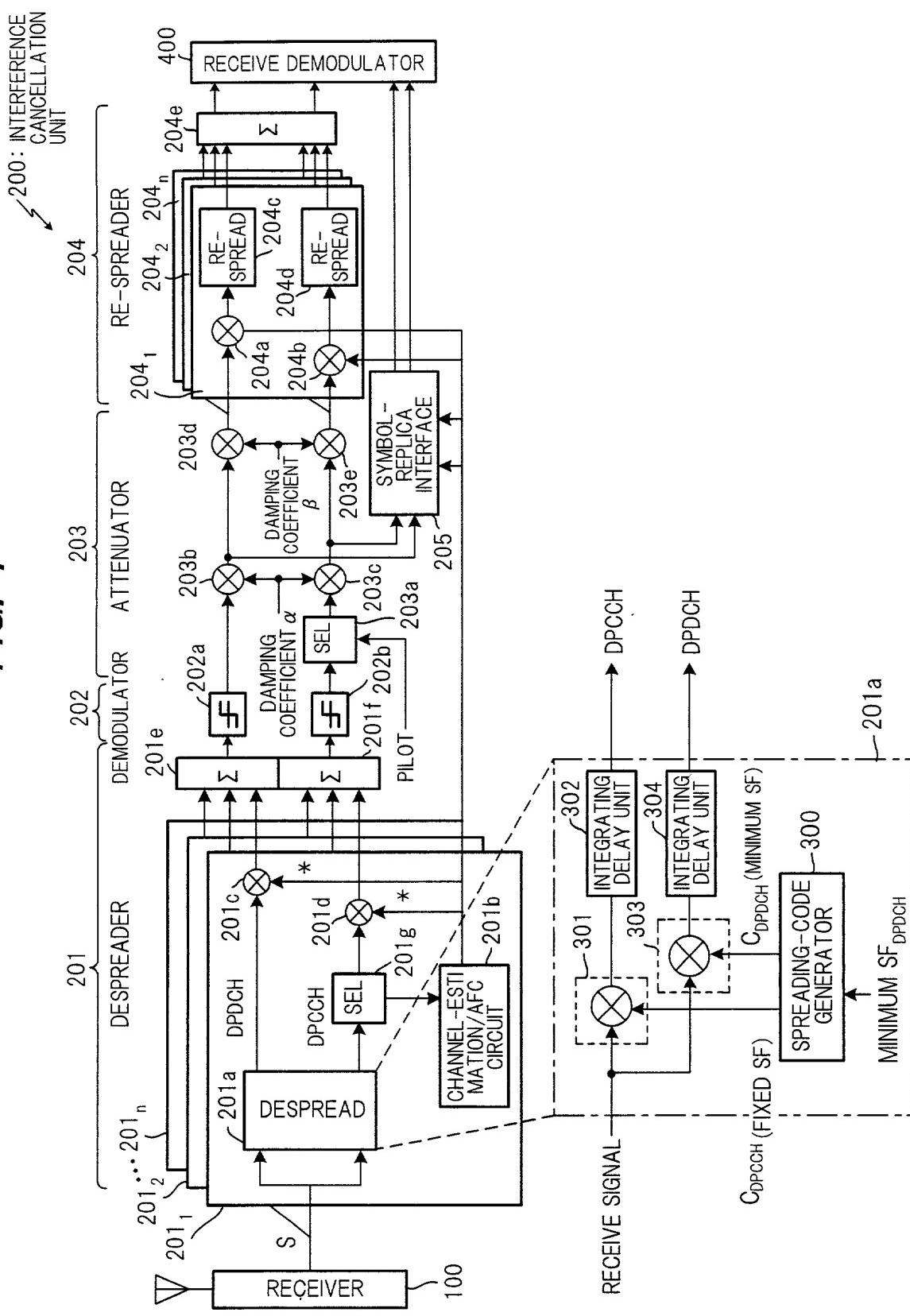


FIG. 1



***FIG. 2***

RECEIVE SIGNAL	DPDCH	SF1	SF2	SF3	SF4	SF5
	DPCCH	SF1	SF1	SF1	SF1	SF1
RECEIVE SIGNAL	DPDCH	SF1	SF2	SF3	SF4	SF5
	DPCCH	SF1	SF1	SF1	SF1	SF1
INTERFERENCE REPLICA	DPDCH	SF5	SF5	SF5	SF5	SF5
	DPCCH	SF1	SF1	SF1	SF1	SF1

↔

1 FRAME

$SF1 > SF2 > SF3 > SF4 > SF5 = \text{MINIMUM SF}$

FIG. 3

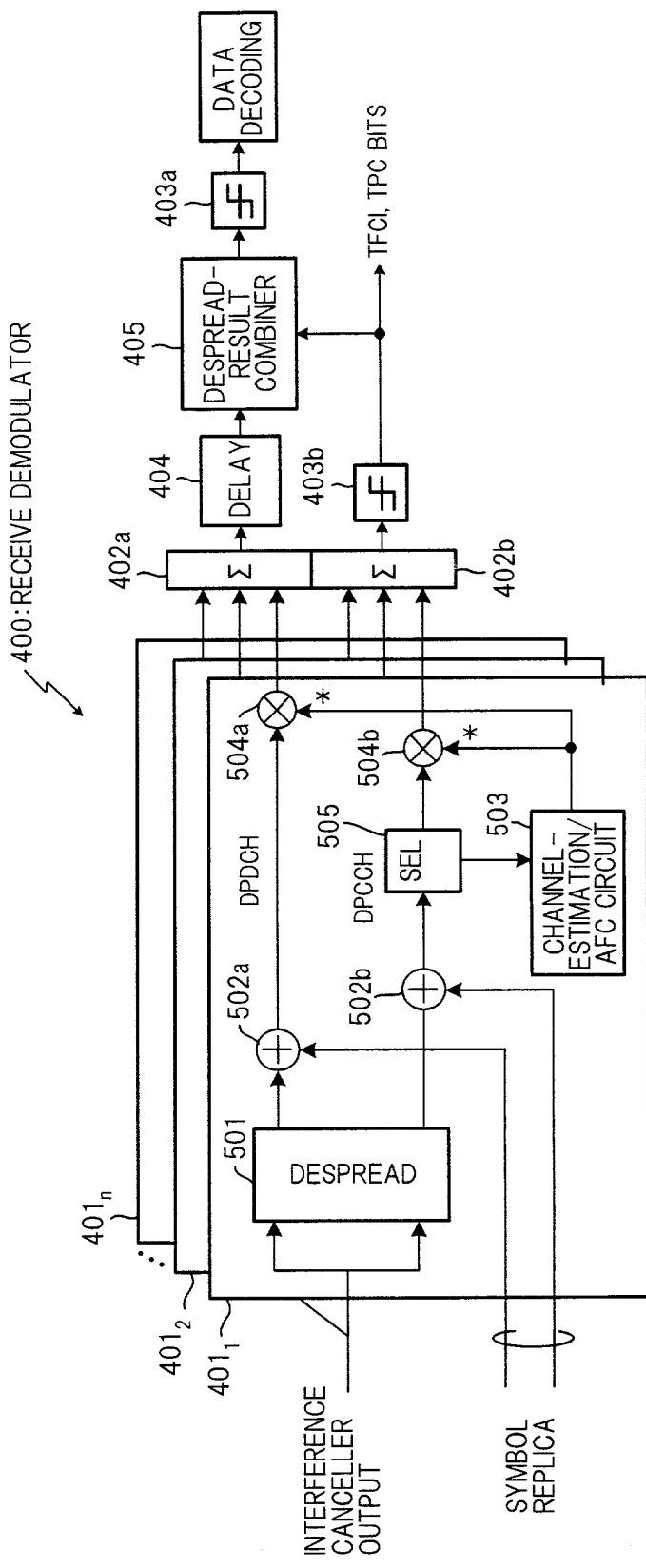


FIG. 4

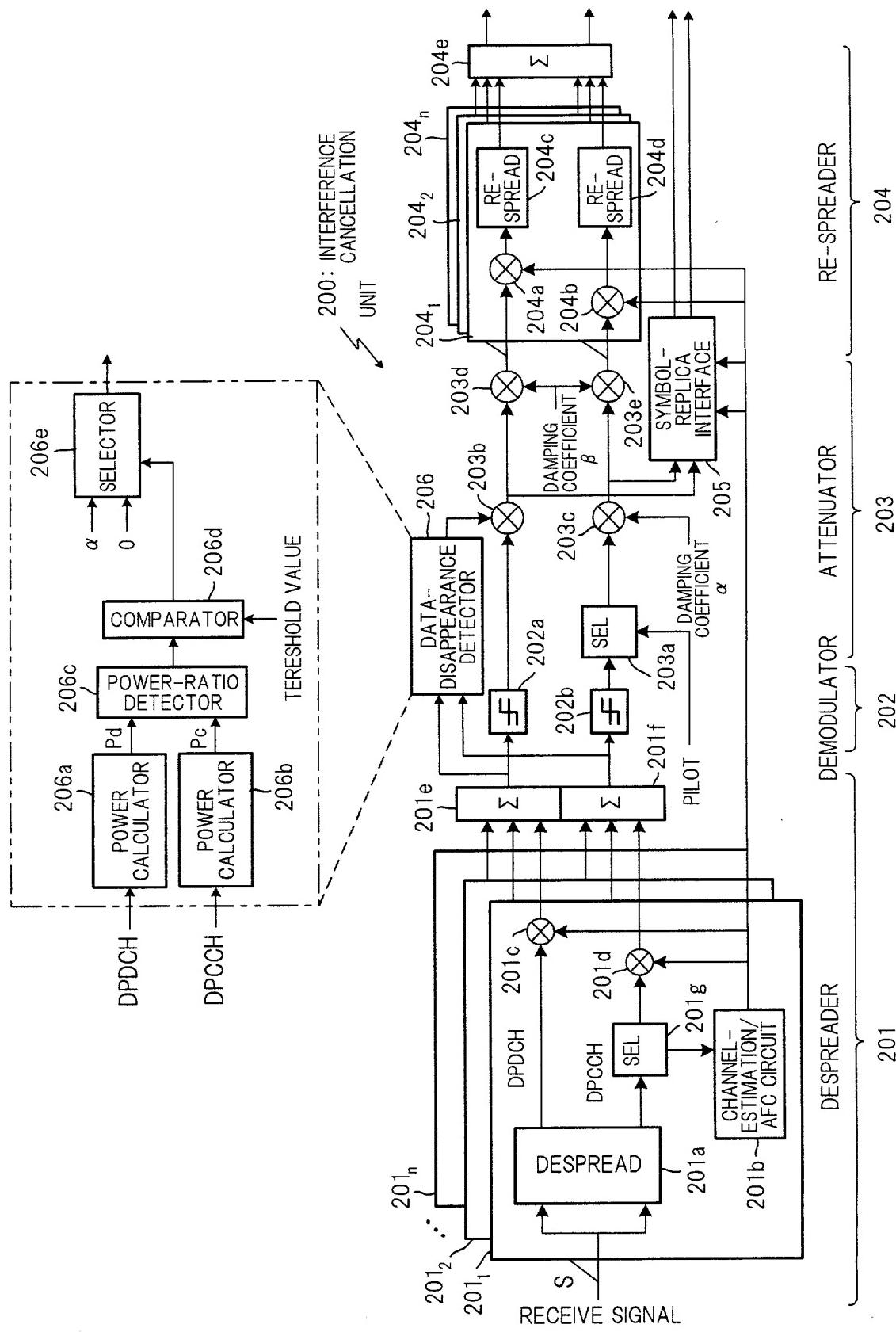


FIG. 5

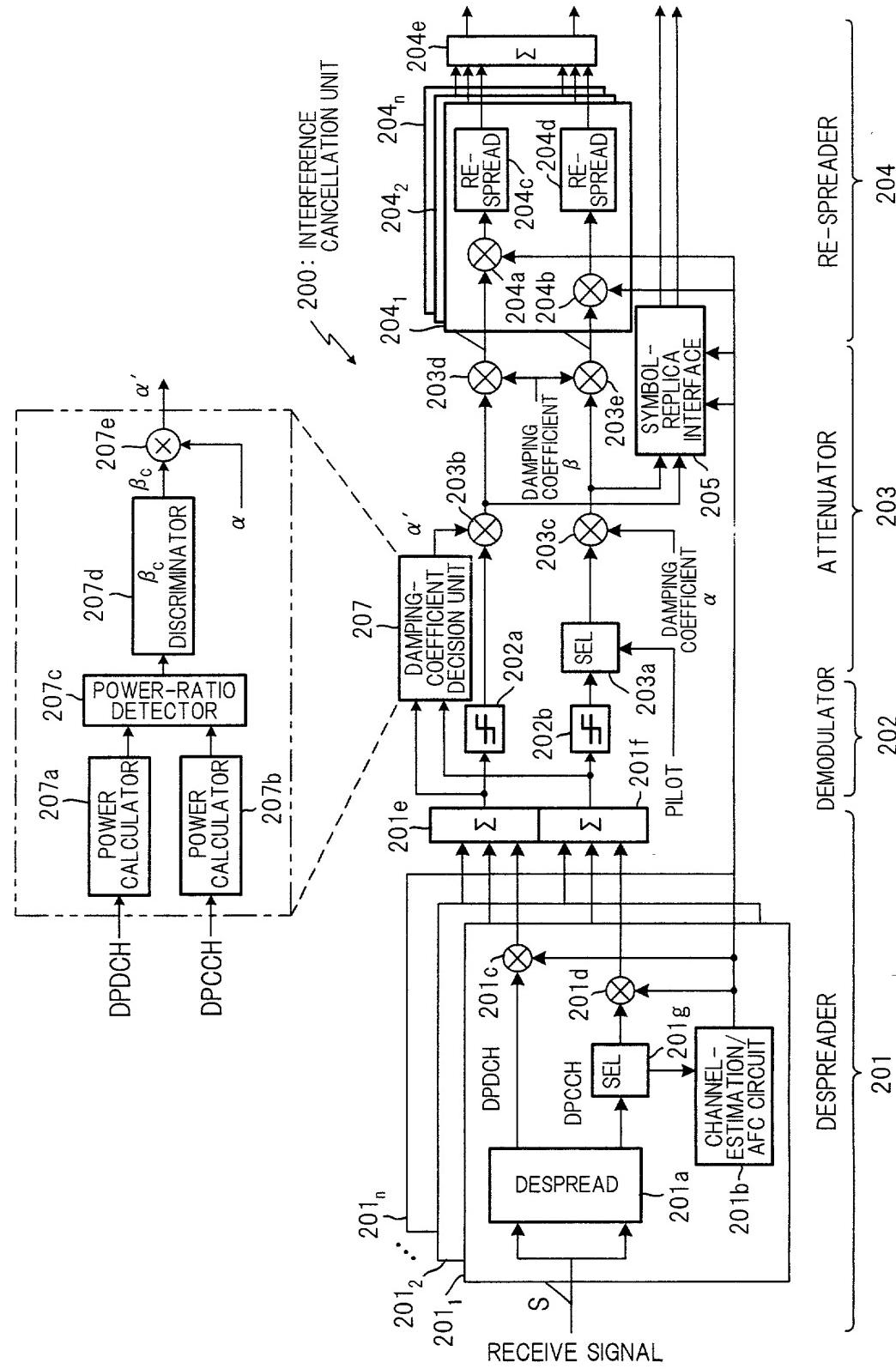
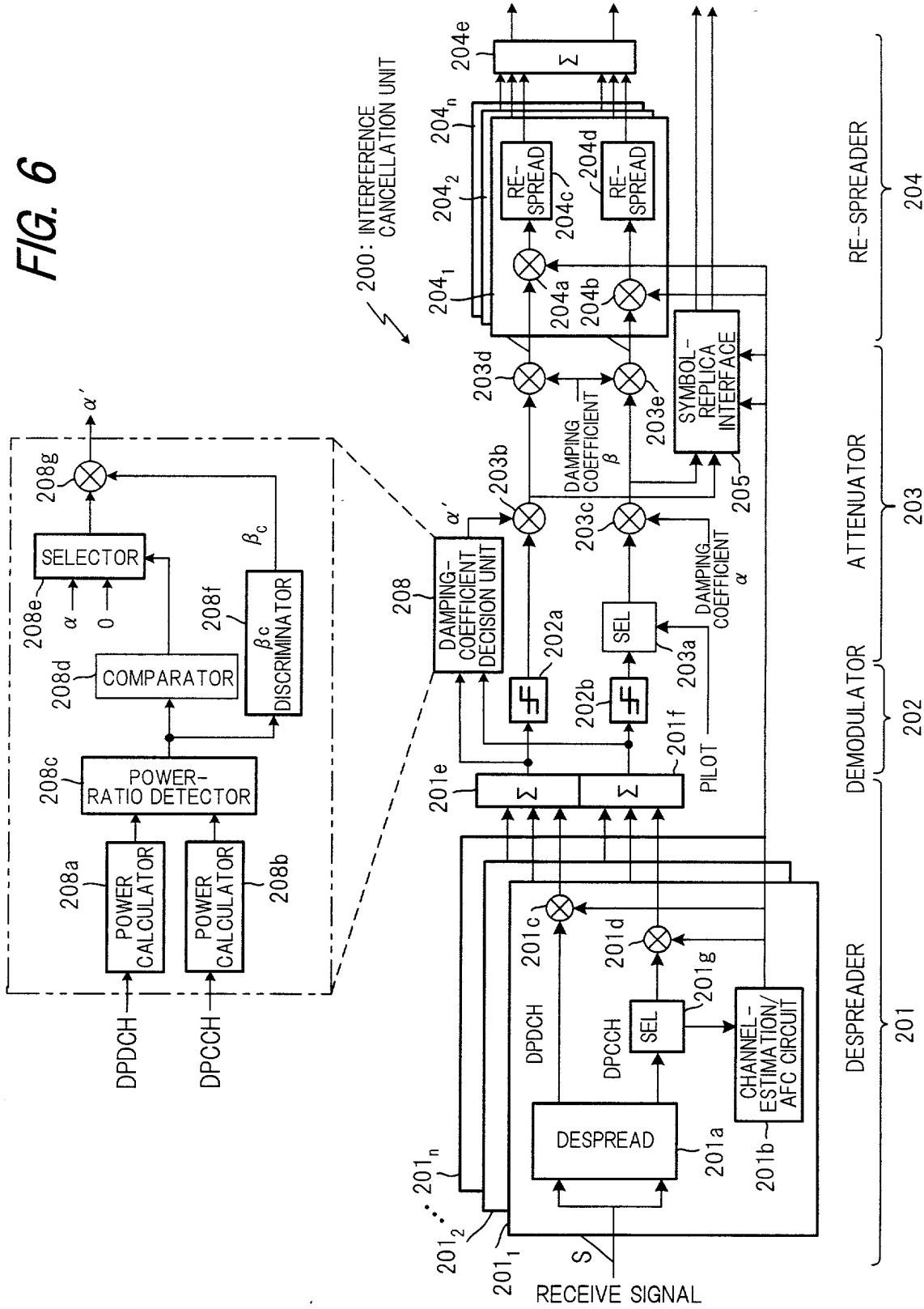
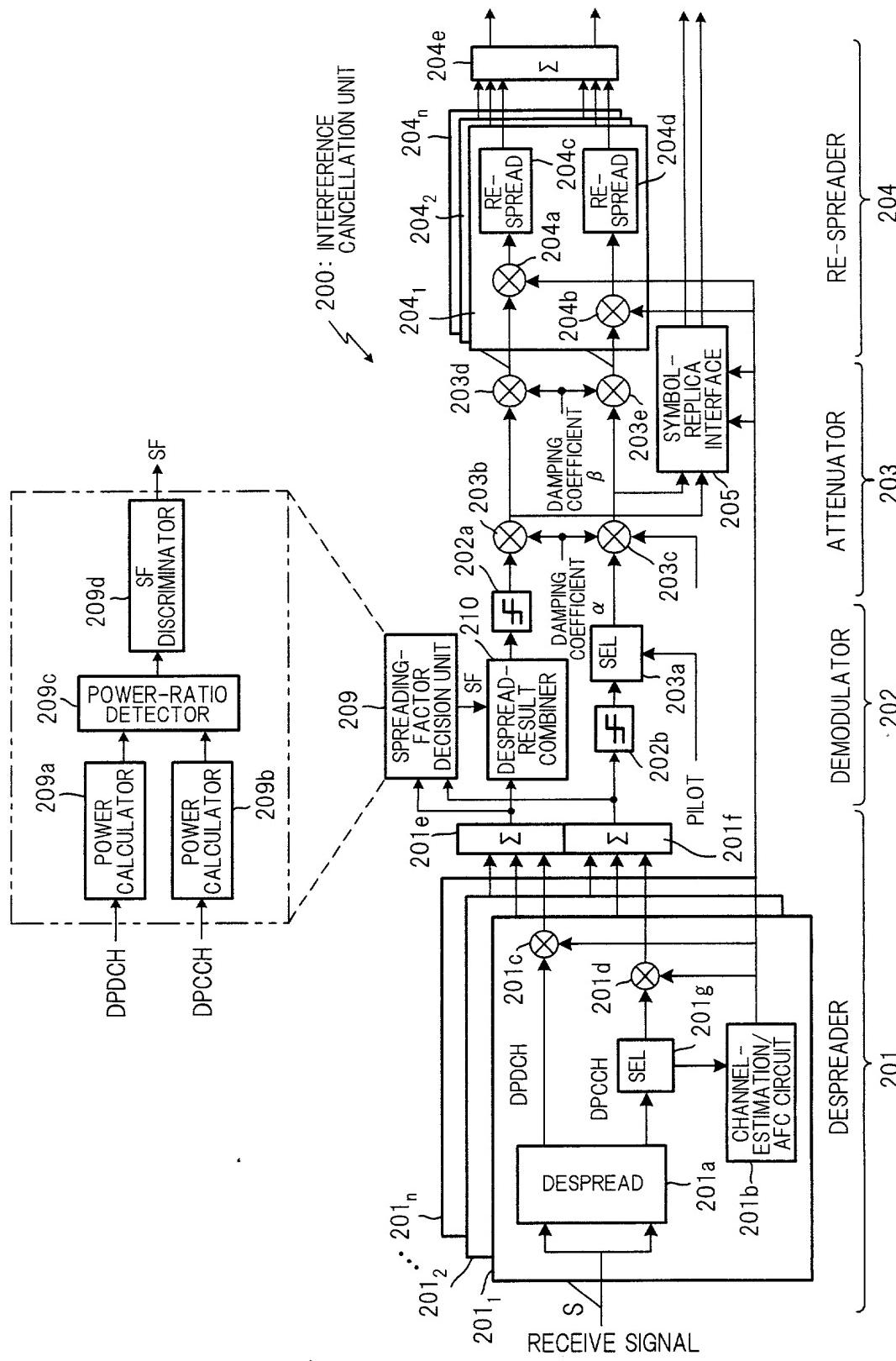


FIG. 6



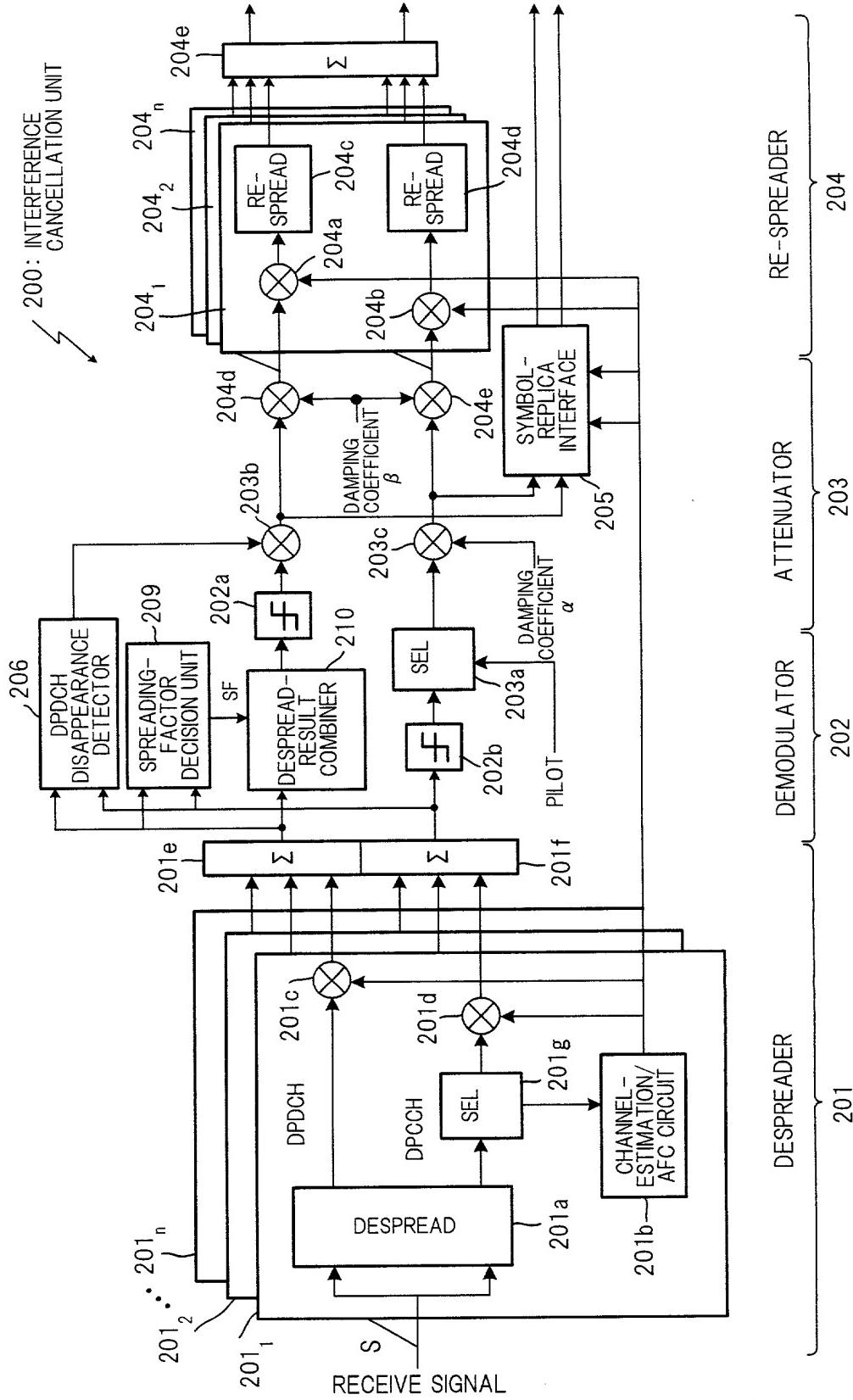
**FIG. 7**

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*FIG. 8*

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*F/G. 9*

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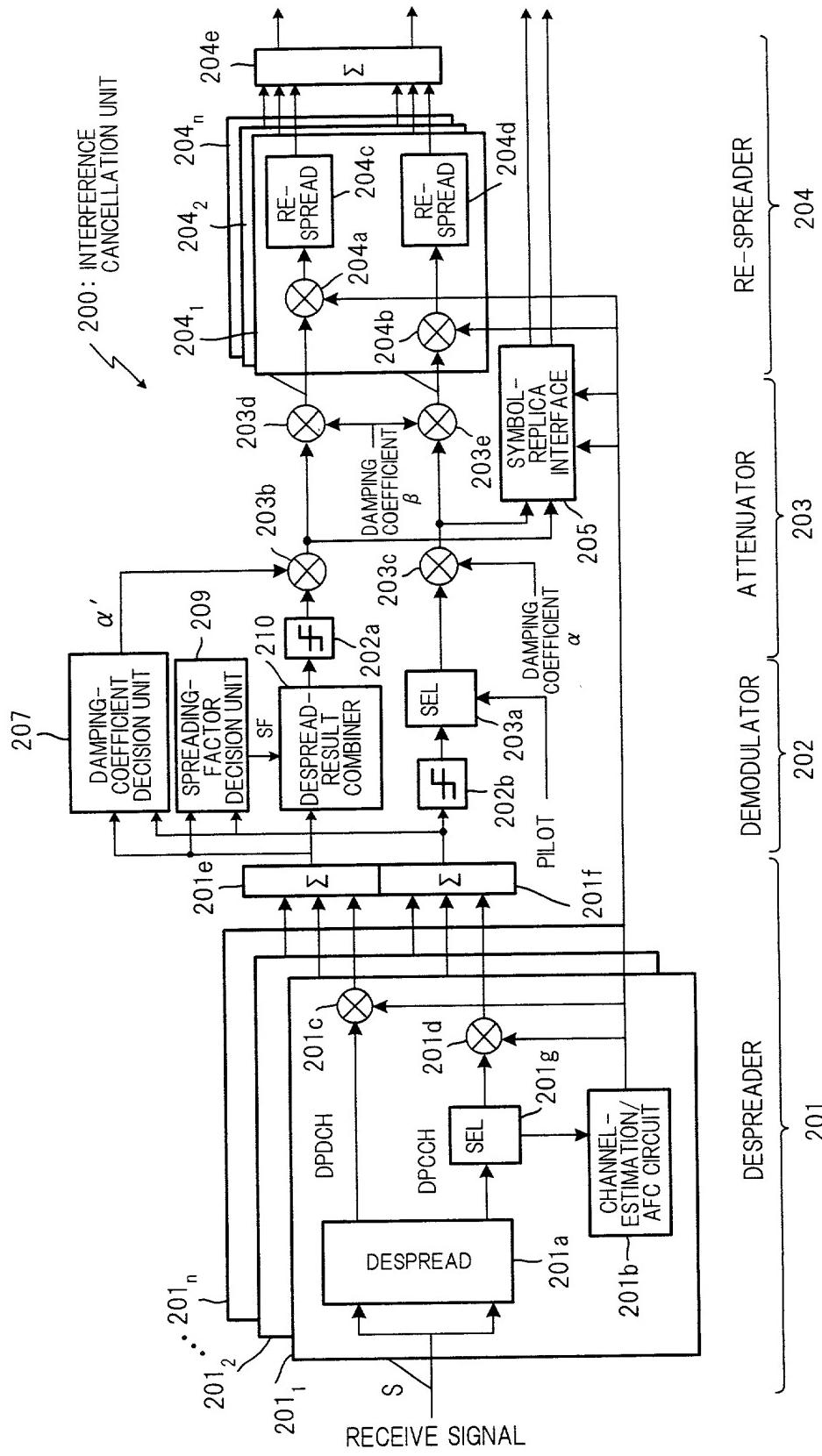


FIG. 10 PRIOR ART

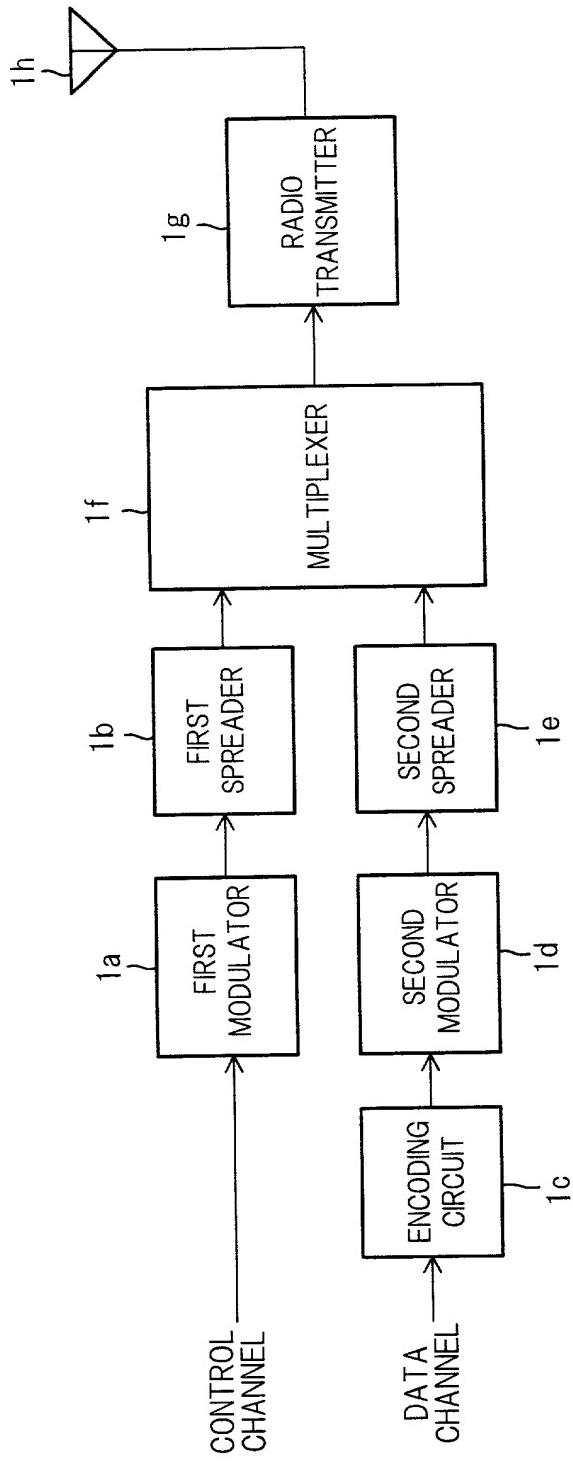


FIG. 11 PRIOR ART

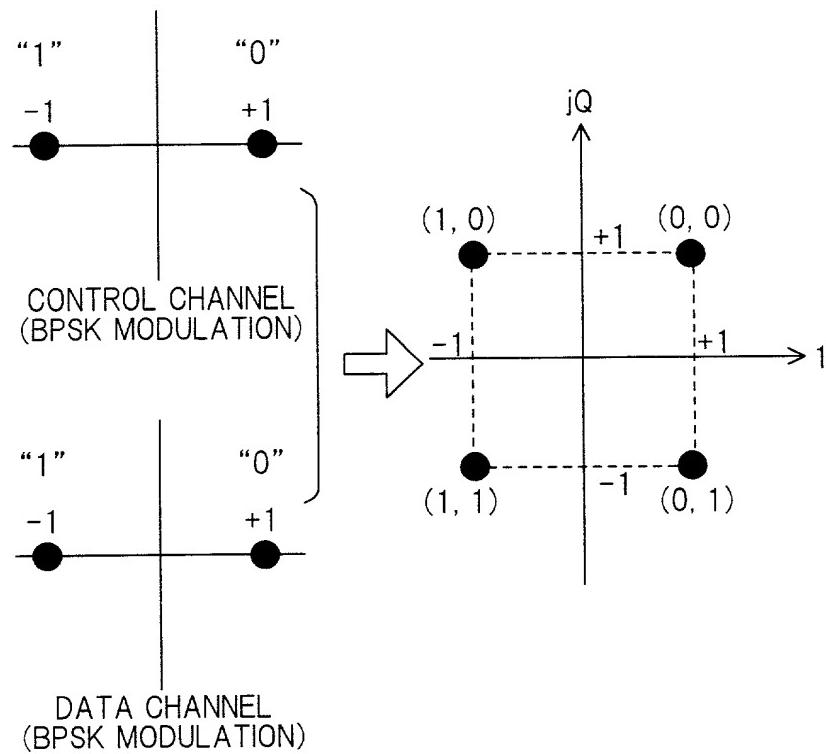


FIG. 12 PRIOR ART

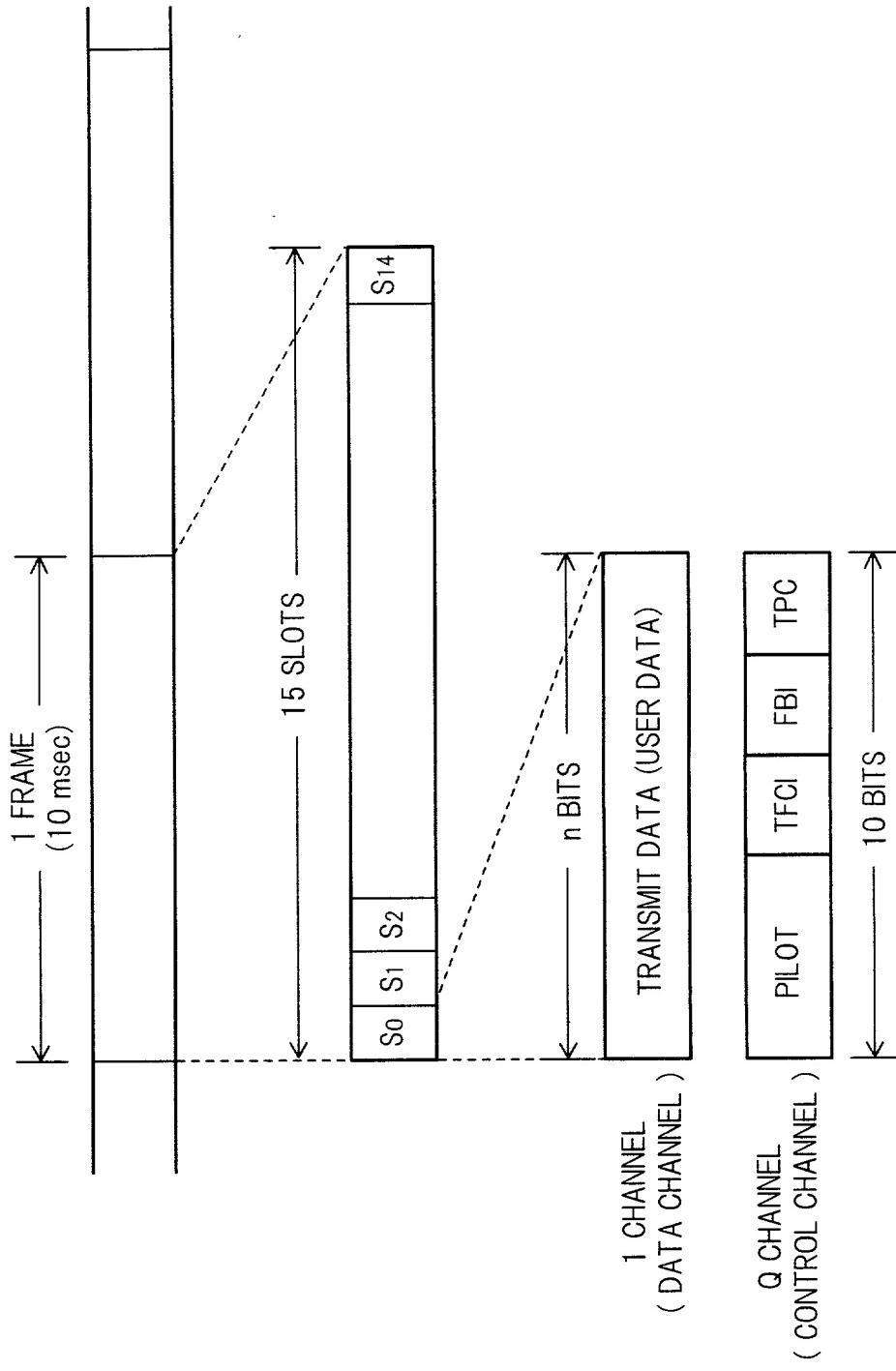
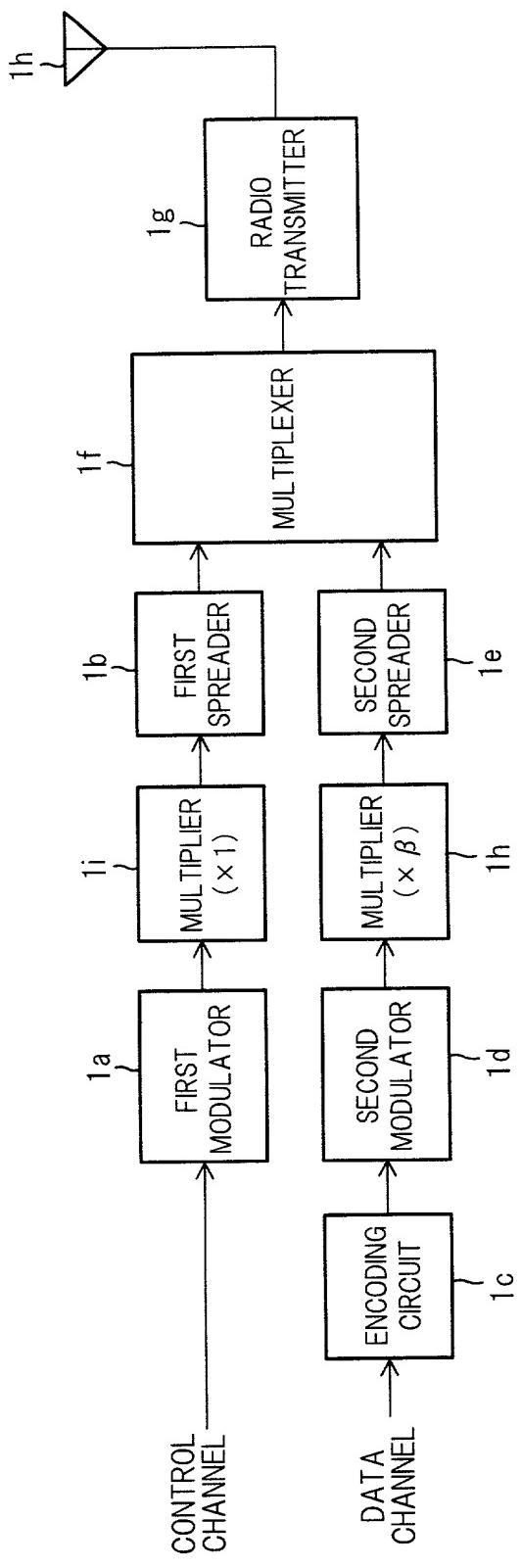


FIG. 13 PRIOR ART



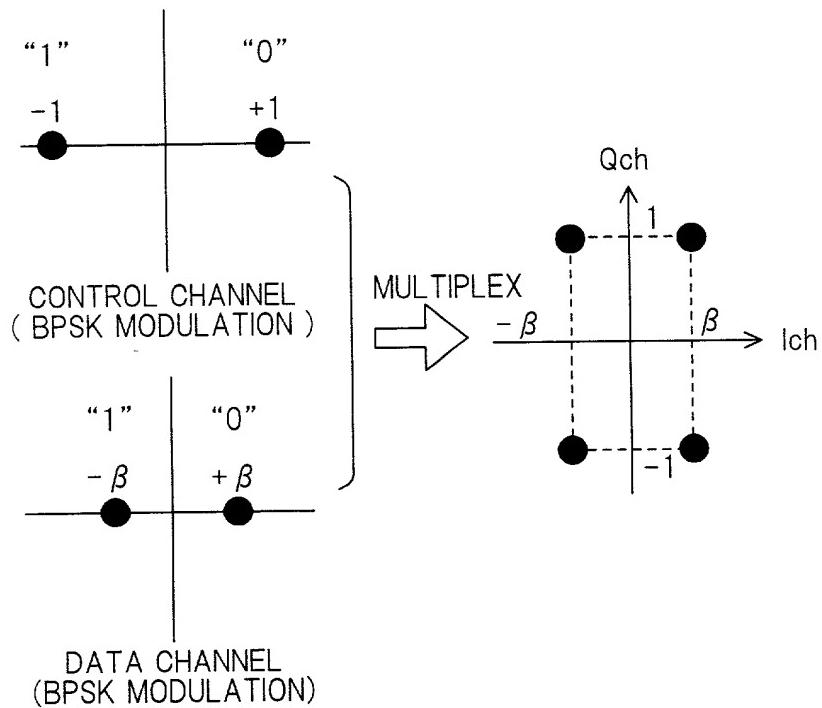
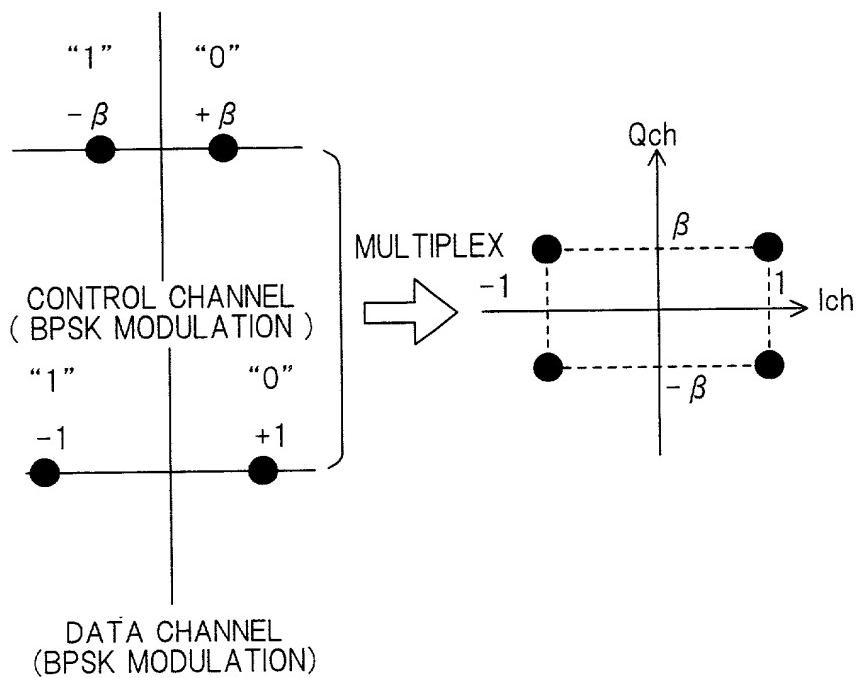
***FIG. 14A PRIOR ART******FIG. 14B PRIOR ART***

FIG. 15 PRIOR ART

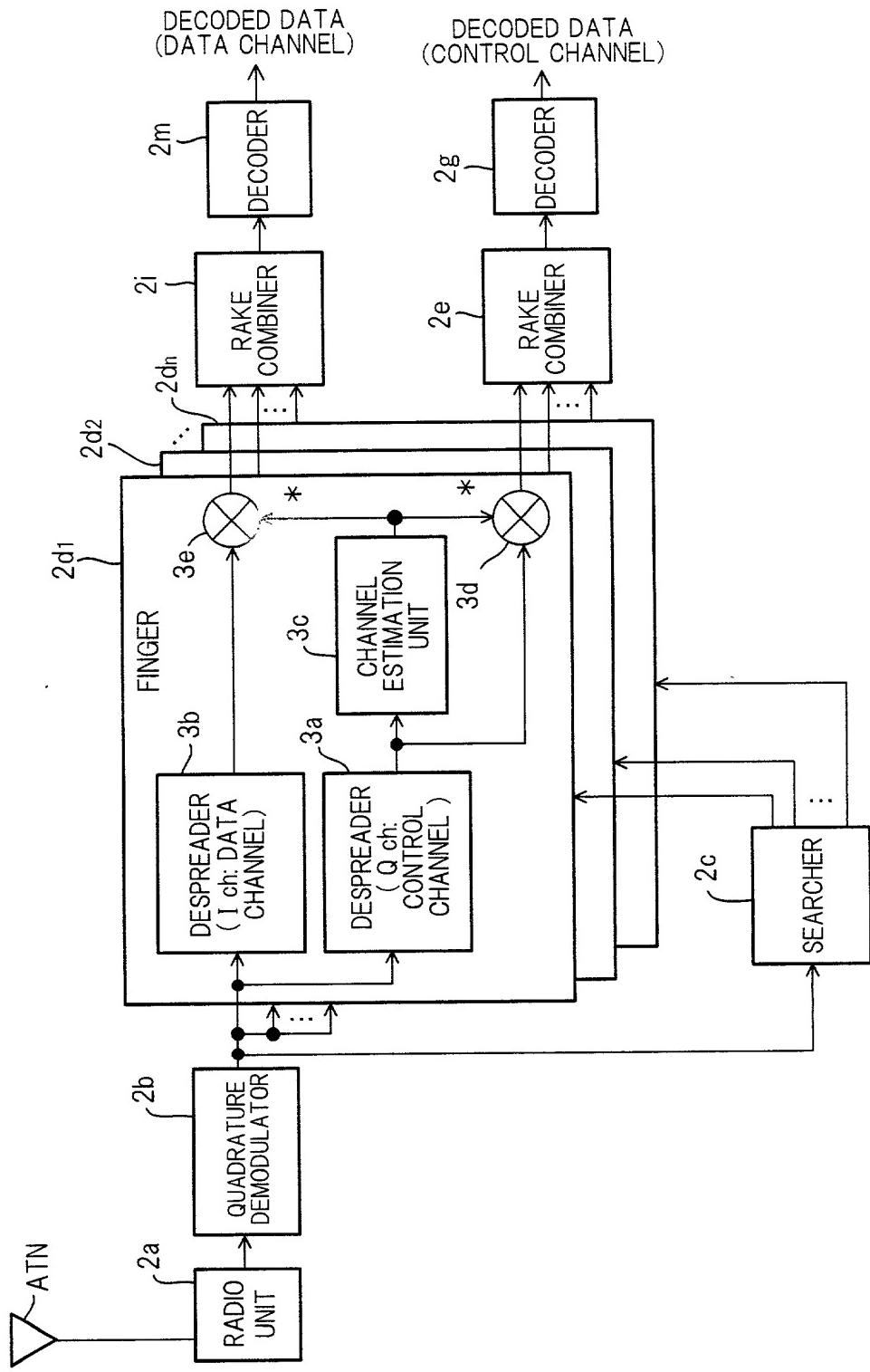


FIG. 16 PRIOR ART

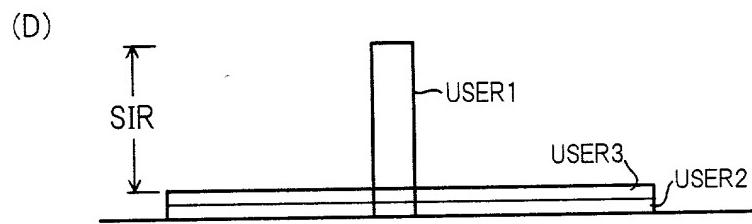
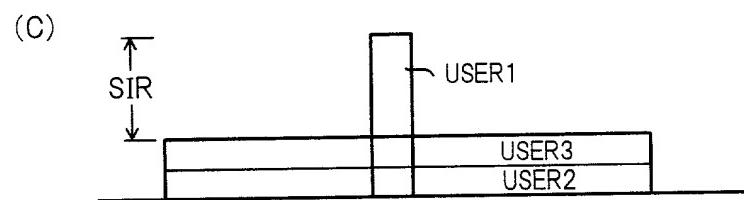
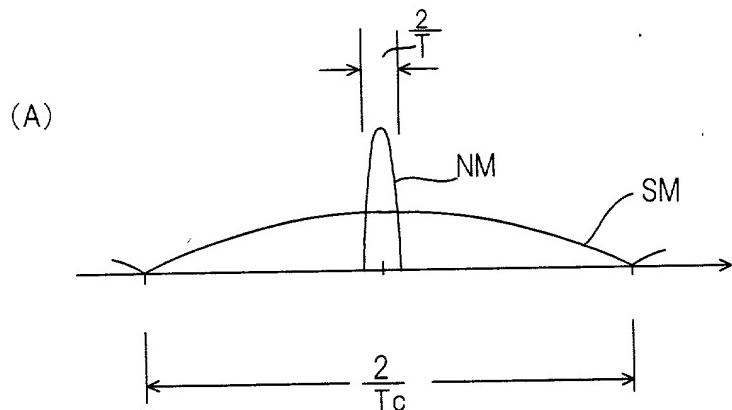


FIG. 17 PRIOR ART

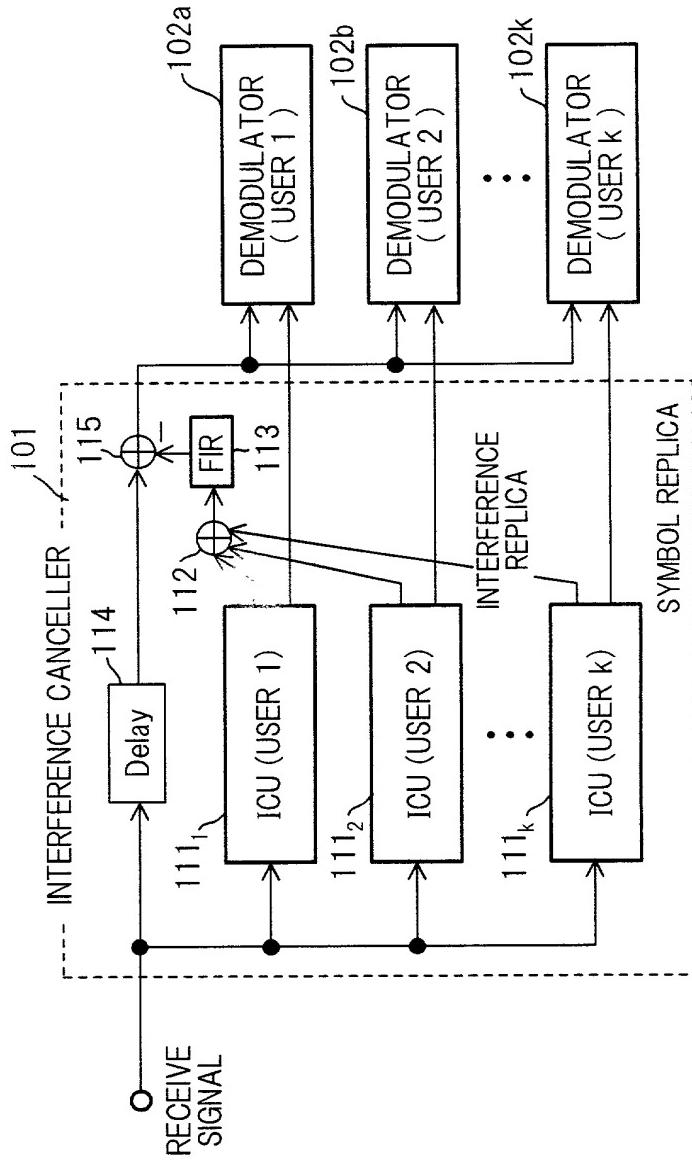
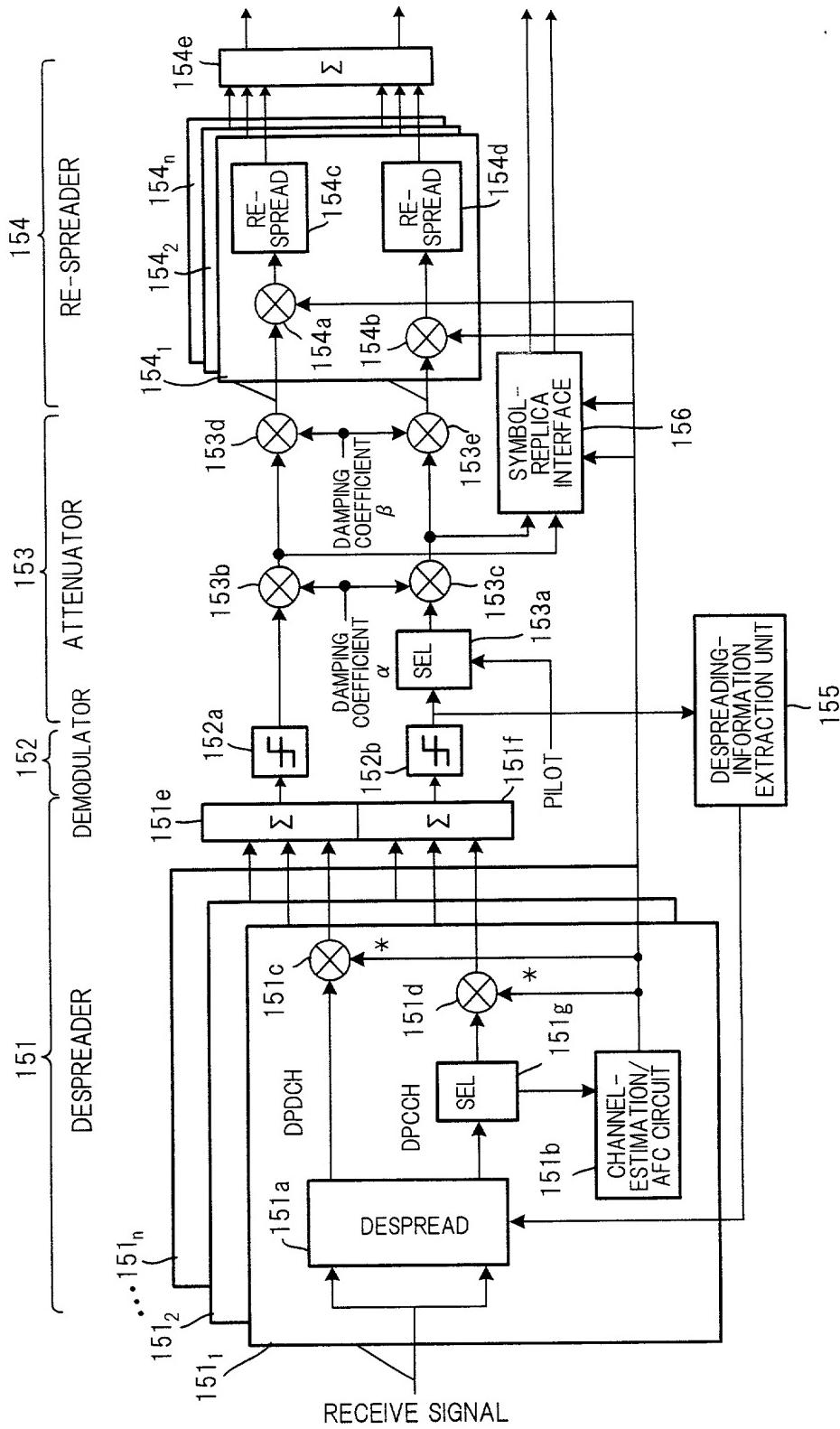
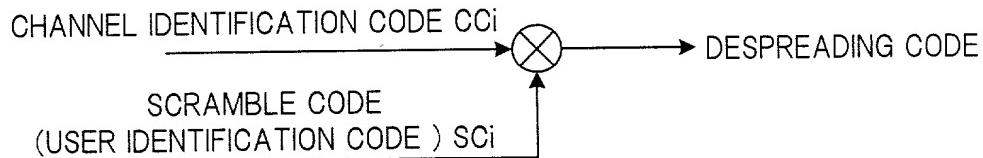
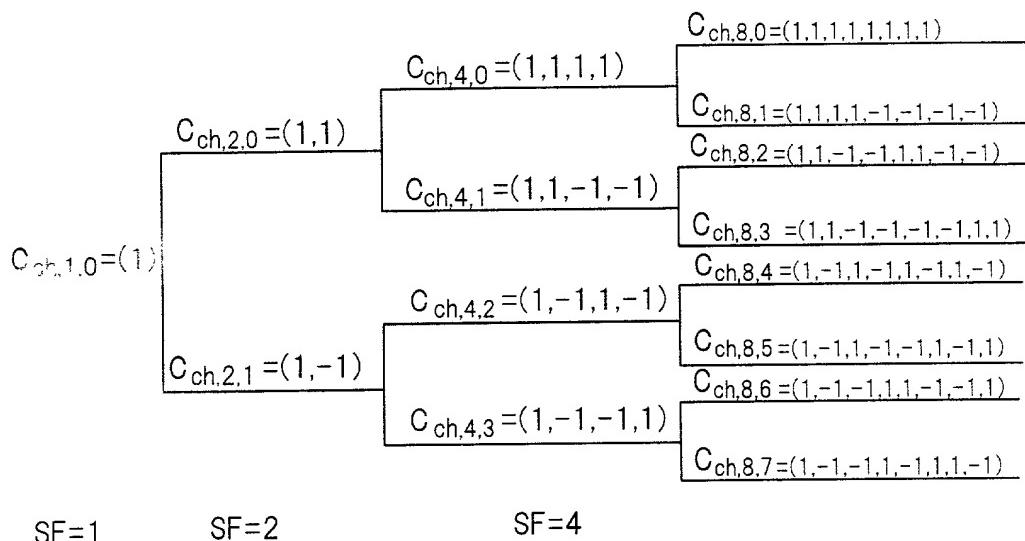


FIG. 18 PRIOR ART



***FIG. 19 PRIOR ART******FIG. 20A PRIOR ART******FIG. 20B PRIOR ART***

$$C_{ch,1,0} = 1$$

$$\begin{bmatrix} C_{ch,2,0} \\ C_{ch,2,1} \end{bmatrix} = \begin{bmatrix} C_{ch,1,0} & C_{ch,1,0} \\ C_{ch,1,0} & -C_{ch,1,0} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{ch,2(n+1),0} \\ C_{ch,2(n+1),1} \\ C_{ch,2(n+1),2} \\ C_{ch,2(n+1),3} \\ \vdots \\ C_{ch,2(n+1),2(n+1)-2} \\ C_{ch,2(n+1),2(n+1)-1} \end{bmatrix} = \begin{bmatrix} C_{ch,2^n,0} & C_{ch,2^n,0} \\ C_{ch,2^n,0} & -C_{ch,2^n,0} \\ C_{ch,2^n,1} & C_{ch,2^n,1} \\ C_{ch,2^n,1} & -C_{ch,2^n,1} \\ \vdots & \vdots \\ C_{ch,2^n,2^n-1} & C_{ch,2^n,2^n-1} \\ C_{ch,2^n,2^n-1} & -C_{ch,2^n,1} \end{bmatrix}$$

## FIG. 21 PRIOR ART

FOR SPREADING FACTOR SF (=16)

SYMBOL DATA CHANNEL IDENTIFICATION CODE	Data1	Data2
	"0011001100110011"	"0011001100110011"

FOR SPREADING FACTOR SF<sub>min</sub> (=4)

SYMBOL DATA CHANNEL IDENTIFICATION CODE	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8
	"0011"	"0011"	"0011"	"0011"	"0011"	"0011"	"0011"	"0011"

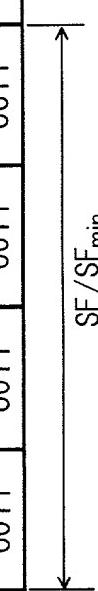
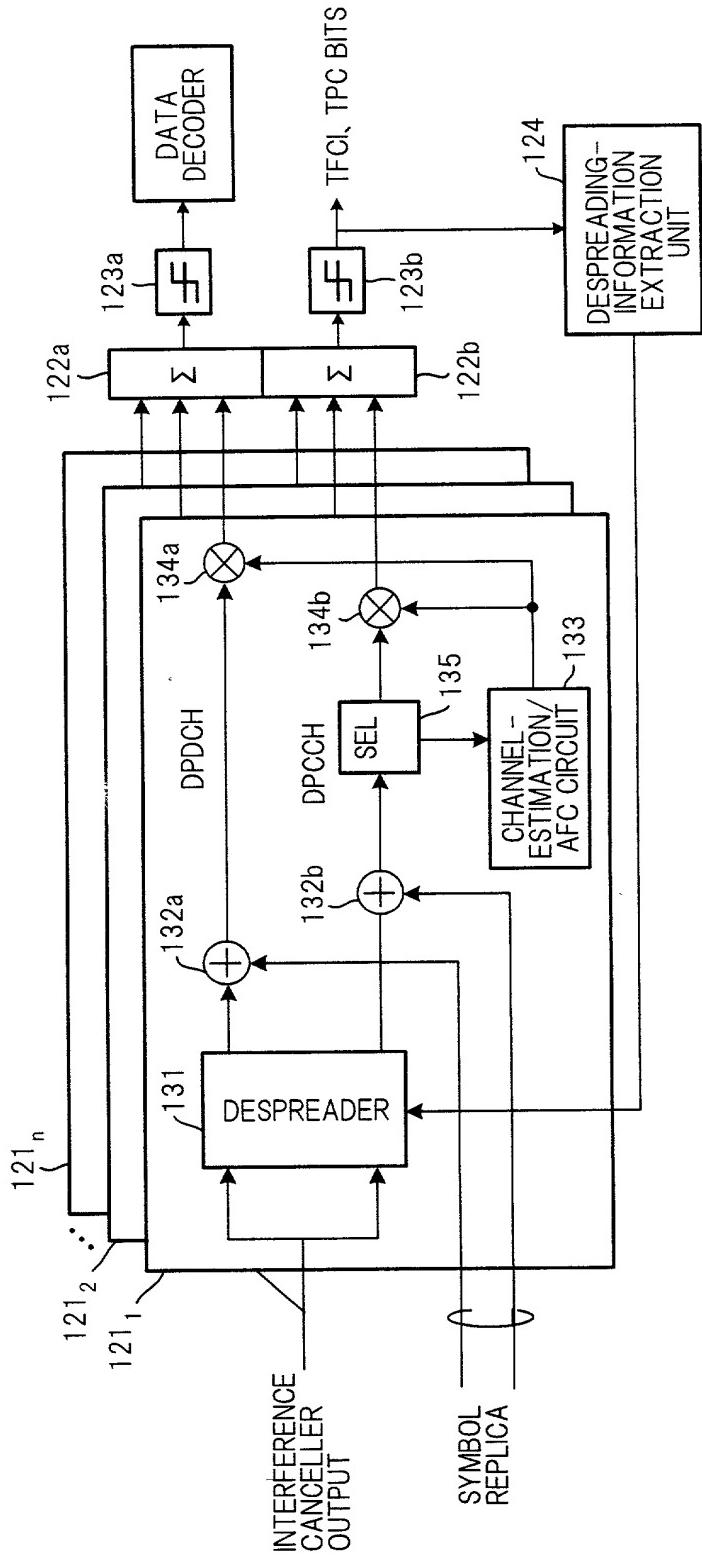
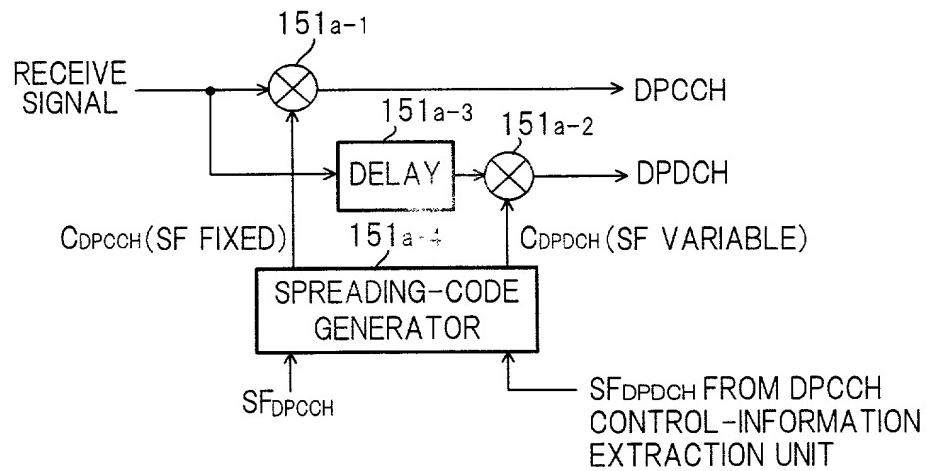


FIG. 22 PRIOR ART



*FIG. 23 PRIOR ART**FIG. 24 PRIOR ART*

RECEIVE SIGNAL	DPDCH	SF1	SF2	SF3	SF4	SF5
	DPCCH	SF1	SF1	SF1	SF1	SF1
DELAYED RECEIVE SIGNAL	DPDCH	SF1	SF2	SF3	SF4	
	DPCCH	SF1	SF1	SF1	SF1	
INTERFERENCE REPLICA	DPDCH	SF1	SF2	SF3	SF4	
	DPCCH	SF1	SF1	SF1	SF1	

↔  
1 FRAME